SPIN TUNNEL TRANSISTOR

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. application Ser. No. 10/926,090, filed Aug. 26, 2004, and is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2003-332103, filed on Sep. 24, 2003, the entire contents of each of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a spin tunnel transistor used for a high-density magnetic recording and reading magnetic head, etc.

[0004] 2. Description of the Related Art

[0005] The recording density in the magnetic recording has been increased at an annual rate of 100 percent since the debut of GMR heads in which the giant magnetoresistive effect (GMR effect) is utilized. A GMR device includes a stacked film having the sandwich structure, Ferromagnetic metal layer/Non-magnetic metal layer/Ferromagnetic metal layer. Taking an example of such device, there is a spin-valve type magnetoresistive device, in which the magnetization of one of the ferromagnetic metal layers is fixed and the magnetization of the other ferromagnetic metal layer is changed according to an external magnetic field. The spin-valve type magnetoresistive device can detect a resistance value incorporating a change in the cosine of the relative angle of magnetization between the ferromagnetic metal layers.

[0006] Further, the development of a TMR device, in which the tunnel magnetoresistive effect (TMR effect) is utilized, is pursued in order to cope with higher density magnetic recording. A TMR device includes a stacked film of Ferromagnetic metal layer/Non-magnetic insulator/Ferromagnetic metal layer. In the TMR device, a voltage is applied between the ferromagnetic metal layers to detect the change in a relative angle of the magnetization between the two ferromagnetic metal layers as a change in tunnel resistance value.

[0007] In cotrast, the development of three-terminal devices, referred to as spin tunnel transistors, is pursued. The device structures thereof include structure of: SMS (Semiconductor/Metal/Semiconductor) type; MIMS (Metal/Insulator/Metal/Semiconductor) type; and MIMIM (Metal/Insulator/Metal/Insulator/Metal) type. However, any of devices having the above structures are double-junction, three-terminal devices. In each of the double-junction, three-terminal devices, a base sandwiched between its emitter and collector is made of a metal (i.e. magnetic stacked film) (see U.S. Pat. No. 5,747,859 for MIMS structure).

[0008] The above-described spin tunnel transistor exhibits an extremely large change of magnetoresistance (MR) of several hundreds percentage, while the collector current is as remarkably small as 10^{-4} times the emitter current and therefore a ratio of collector current to emitter current (i.e. current transmittance) cannot increase. A remarkably small current transmittance is not suitable from the viewpoints of electric power consumption, working speeds, noises, etc.

SUMMARY OF THE INVENTION

[0009] The present invention provides a spin tunnel transistor comprising: a collector; an emitter; a base formed between the collector and the emitter, including a first ferromagnetic metal layer variable in its magnetization under an external magnetic field; a barrier layer formed between the base and one of the collector and the emitter, the other of the collector and the emitter including a semiconductor crystal layer; and a transition metal silicide crystal layer between the semiconductor crystal layer and the base. The transition metal silicide crystal layer may be replaced with a palladium layer, a transition metal nitride layer, or a transition metal carbide layer.

[0010] In regard to a spin tunnel transistor with a magnetic stacked film used for its base section, in a base-collector interface is interposed a thin transition metal silicide crystal layer, a transition metal nitride layer, a transition metal carbide layer or a Pd layer, whereby a spin tunnel transistor with a large MR ratio and a large current transmittance can be achieved.

[0011] Each of these spin tunnel transistors may be formed/used as a magnetic reproducing sensor or sensing element of a magnetic reproducing head. Also, each of these spin tunnel transistors may be formed/used as a memory element of integrated memory circuit, such as a magnetic random access memory.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] **FIG. 1** is a cross-sectional diagrammatic illustration of assistance in explaining a spin tunnel transistor according to the first embodiment of the invention;

[0013] **FIG. 2** is an energy diagram of the spin tunnel transistor according to the first embodiment; and

[0014] **FIG. 3** is a cross-sectional diagrammatic illustration of assistance in explaining a spin tunnel transistor according to the second embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] The embodiments of the invention will be described in reference to the drawings below.

[0016] Constituent features common throughout the embodiments and examples are identified by the same reference character and the redundancy of the description thereof is omitted. Each of the drawings is a diagrammatic illustration for facilitating the description and understanding of the invention. Some of shapes, dimensions, ratios, etc. illustrated in the drawings differ from corresponding ones in the actual device, but these may be changed in design appropriately in consideration of the following description and the known art.

Embodiment 1

[0017] A spin tunnel transistor in connection with the first embodiment of the invention will be described in reference to the cross-sectional diagrammatic illustration of **FIG. 1**.